REMARKS/ARGUMENT

The Examiner has determined that the title of the invention is not descriptive. By this amendment the title has been amended from "WRITE BACK POLICY FOR MEMORY BASED ON STACK TREND INFORMATION" to instead be --DIRTY CACHE LINE WRITE BACK POLICY BASED ON STACK SIZE TREND INFORMATION--. Applicants believe this to be more descriptive of their invention that the title suggested by the Examiner.

Objected to Claims 7, 9, 15 and 16 have been amended to be in independent form, including all of the limitations of the base claim and any intervening claims. Accordingly, Claims 7, 9, 10, 15 and 16 stand allowable.

Independent Claim 1 has been amended better to define the claimed invention and overcome the 35 U.S.C. 112, first paragraph, rejection. Accordingly, the 35 U.S.C. 112, first paragraph, rejection of Claims 1-10 is overcome.

1) Claims 1-4, 8, 11 and 13 stand rejected under 35 U.S.C. 102(b) as being unpatentable over Shen et al. (U.S. Patent 5,687,336) (hereinafter "Shen"). Applicants respectfully traverse this rejection as set forth below.

In order that the rejection of Claims 1-4, 8, 11 and 13 be sustainable, it is fundamental that "each and every element as set forth in the claim be found, either expressly or inherently described, in a single prior art reference." *Verdegall Bros. v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). See also, *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989), where the court states, "The identical invention must be shown in as complete detail as is contained in the ... claim".

Furthermore, "all words in a claim must be considered in judging the patentability of that claim against the prior art." *In re Wilson*, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970).

Independent Claim 1 requires and positively recites, a method of managing memory, comprising: "**determining stack trend information** using current and future stack operating instructions" and "utilizing **the trend information to reduce data traffic between various levels of a memory**".

Independent Claim 11 as amended, requires and positively recites, a computer system, comprising: "a processor; a memory coupled to the processor", "a stack that exists in memory and contains stack data", "a memory controller coupled to the memory", "**trend logic**", "wherein the processor executes instructions", "wherein the **trend logic provides trend information about the stack to the controller**" and "wherein the **trend information about the stack is based on at least one future instruction**".

In contrast, Shen discloses:

> An instruction is first decoded in the D stage instruction decoder 16. Fields in the instruction can indicate which registers in register file 10 are accessed by the instruction. For stack-type instructions, stack pointer 12 (SP) is read from register file 10 and inputted to first adder 18 (col. 4, lines 11-15).
>
> FIG. 2 is an improvement in a pipelined processor for executing multiple stack instructions in the pipeline. Decode 16, register file 10, and memory 26 operate as described for FIG.1. Pipeline valid bits 50 indicate the locations of valid stack instructions in the pipeline. From the locations for the stack instructions from valid bits 50, increment logic 20 determines increment value 94 to add to stack pointer 12 stored in register file 10. If older stack instructions exist in the pipeline, an additional amount of increment value 94 is added by logic 20 to account for the older stack instructions in the pipeline.

> Three-port adder 40 is used to generate the address of the top of the stack (TOS) directly without calculating the new stack pointer. The old stack pointer 12 from register file 10, along with the increment amount from increment logic 20 and the segment base address 24 are added together without having to generate the new stack pointer.
>
> The new stack pointer SP' is not generated until the end of the pipeline, when the new stack pointer is written to register file 10. Final increment logic 20' generates increment value 94 for the instruction at the end of the pipeline, which is added to stack pointer 12 in final adder 42 to generate the new stack pointer SP'. Thus the updated stack pointer need only be generated at the end of the pipeline. Timing of Multiple Stack Instructions in Pipeline (col. 4, lines 36-60).

Contrary to Examiner's determination, there is no teaching whatsoever in the above that indicates whether the stack size has increased or decreased. The only way that Examiner can reach such a conclusion is if he is comparing in his mind the new stack pointer with the previous stack pointer and then making a further assumption that it somehow reflects an increase or decrease in stack size. Shen provides no such leap in logic. There is simply no teaching in the above Examiner-referenced sections of Shen for ""**determining stack trend information . . .**", as required by Claim 1. Morevoer, even if, arguendo, Shen has a stack point that may change from time to time – it reflects a "change", not the "trend" of such change. Examiner has provided no evidence from Shen that a change in its stack pointer reflects a "trend" in the change. In other words, by changing its pointer, Shen reflects that a change has occurred, but it indicates nothing about any "trend" that can be interpreted from the change. Accordingly, Examiner's determination is supposition not supported by fact and little more than improper hindsight reconstruction.

Further, while Shen may well disclose "increment logic" (col. 4, lines 40-43; Fig. 2, element 20) there is no teaching in Shen that its "increment logic" also determines "trends" in the logic. Accordingly, Examiner's determination is supposition not supported by fact and little more than improper hindsight reconstruction. Shen simply does not teach or suggest, "**trend** logic", as required by Claim 11.

Similarly, even if, arguendo, Shen discloses a stack pointer that signals a "mis-aligned access", such determination is not indicative of a "trend" – but a single occurrence. Whether or not Shen uses idenfication of a mis-aligned access to prevent a push-pop pairing is irrelevant to the present claim language. Moreover, even if the result of such one-time determination is used to prevent a push/pop pairing, such reduction in data traffic is NOT a result of "utilizing **the trend information to reduce data traffic between various levels of a memory**", as required by Claim 1 OR "wherein the **trend logic provides trend information about the stack to the controller**", as required by Claim 11.

Further, since Shen fails to teach or suggest a device that discloses "trend" information, if further fails to teach or suggest, "wherein the **trend information about the stack is based on at least one future instruction**", as further required by Claim 11.

In light of the above it is clear that "each and every element as set forth in claims 1 and 11 cannot be found, either expressly or inherently described, in a single prior art reference", as required by law. Accordingly, the 35 U.S.C. 102(b) rejection of Claims 1 and 11 over Shen is improper and must be withdrawn.

Applicants further point out that Examiner makes two improper "inherency" arguments against Claim 11.

First, Examiner agrees that Shen does not disclose a memory controller in its design (Office action, page 5, lines 17-18). Yet Examiner goes on to argue, without providing any extrinsic evidence to support his argument, that one of ordinary skill in the art knows a memory controller is inherently required to interface with any memory.

Second, Examiner relies upon his first inherency argument above (that a memory controller is required to interface with any memory) to make a second inherency argument that Shen discloses that "trend" information is sent to the memory controller. Examiner's double inherency argument is improper.

"To establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill.' ... 'Inherency however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient". *In re Robertson*, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999). "In relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art." *Ex parte Levy*, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Int'f 1990). "A prior art reference anticipates a claim only if the reference discloses, either expressly or inherently, every limitation of the claim."; "About the most that can be said for the [prior art] patent is that it does not explicitly describe anything inconsistent with [the claimed] procedures. However, this negative pregnant is no enough to show anticipation." *Rowe v. Dror*, 112 F.3d 473, 478, 480-81, 42 USPQ2d 1550, 1553, 1555 (Fed. Cir. 1997). Summary judgment of inherency anticipation was improper because of a material fact issue whether a prior art reference's process necessarily produced the claimed invention's features; "To serve as an anticipation when the reference is silent about the asserted inherent characteristic, such gap in the reference

may be filled with recourse to extrinsic evidence. Such evidence must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill". *Continental Can Company USA, Inc. v. Monsanto Co.*, 948 F.2d 1264, 1269, 20 USPQ2d 1746, 1749-50 (Fed. Cir. 1991).

Claims 2-4 and 8 stand allowable as depending directly, or indirectly, from allowable Claim 1. Claim 13 stands allowable as depending indirectly from allowable Claim 11.

Claim 2 further defines the method of claim 1, wherein determining the trend information includes examining future instructions to determine if the size of the stack is going to decrease as a result of future instructions. Claim 2 is allowable for the same reasons set forth above in support of the allowance of Claim 1. Further, since Shen does not teach or suggest "determining trend information", it similarly fails to further teach or suggest, trend information that "includes examining future instructions to determine if the size of the stack is going to decrease as a result of future instructions". There is no support in the locations in Shen cited by the Examiner (col. 3, line 65 – col. 7, line 7; col. 4, lines 11-15 and 36-60; col. 5, lines 1-5 and 9-10; and Fig. 2) that anticipate the additional elements of Claim 2. Accordingly, the 35 U.S.C. 102(b) rejection of Claim 2 over Shen is improper and must be withdrawn.

Claim 3 further defines the method of claim 2, wherein a predetermined number of instructions are used in determining stack trend information. Claim 3 is allowable for the same reasons set forth above in support of the allowance of Claim 2. Claim 2 is allowable for the same reasons set forth above in support of the allowance of Claim 1. Further, since Shen does not teach or suggest "determining trend information" that "includes examining future instructions to determine if the size of the stack is going to

decrease as a result of future instructions", it does NOT further teach or suggest, "wherein a predetermined number of instructions are used in determining stack trend information". There is no support in the locations in Shen cited by the Examiner (col. 3, lines 65-67 and col. 6, lines 47-48) that anticipate the additional elements of Claim 3. Accordingly, the 35 U.S.C. 102(b) rejection of Claim 3 over Shen is improper and must be withdrawn.

Claim 4 further defines the method of claim 3, wherein the number of predetermined instructions is at least two. Claim 4 is allowable for the same reasons set forth above in support of the allowance of Claim 3. Claim 3 is allowable for the same reasons set forth above in support of the allowance of Claim 2. Claim 2 is allowable for the same reasons set forth above in support of the allowance of Claim 1. Further, since Shen does not teach or suggest "determining trend information" that "includes examining future instructions to determine if the size of the stack is going to decrease as a result of future instructions", "wherein a predetermined number of instructions are used in determining stack trend information", it does NOT further teach or suggest, "wherein the number of predetermined instructions is at least two". There is no support in the locations in Shen cited by the Examiner (col. 3, lines 65-67 and col. 6, lines 47-48) that anticipate the additional elements of Claim 4. Accordingly, the 35 U.S.C. 102(b) rejection of Claim 4 over Shen is improper and must be withdrawn.

Claim 8 further defines the method of claim 1, wherein determining the trend information includes examining future instructions to determine if the size of the stack is going to increase as a result of future instructions. Claim 8 is allowable for the same reasons set forth above in support of the allowance of Claim 1. Further, since Shen does not teach or suggest "determining trend information", it similarly fails to further teach or suggest, "wherein determining the trend information includes examining future instructions to determine if the size of the stack is going to increase as a result of future

instructions". There is no support in the locations in Shen cited by the Examiner (col. 3, line 65 – col. 7, line 7; col. 4, lines 11-15 and 36-60; col. 5, lines 1-5 and 9-10; and Fig. 2) that anticipate the additional elements of Claim 8. Accordingly, the 35 U.S.C. 102(b) rejection of Claim 8 over Shen is improper and must be withdrawn.

Claim 13 further defines the computer system of claim 12, wherein the trend logic determines a net stack trend based on current instruction and future instruction information coming from the decoder. Claim 13 is allowable for the same reasons set forth above in support of the allowance of Claim 11. Further, since Shen does not teach or suggest "trend logic", "wherein the processor executes instructions", "wherein the trend logic provides trend information about the stack to the controller" and "wherein the trend information about the stack is based on at least one future instruction", as required by Claim 11, it similarly fails to further teach or suggest, trend information that "wherein the trend logic determines a net stack trend based on current instruction and future instruction information coming from the decoder". There is no support in the locations in Shen cited by the Examiner (col. 3, line 65 – col. 7, line 7; col. 4, lines 11-15; col. 4, lines 11-15; col. 4, lines 36-60; and Fig. 2) that anticipate the additional elements of Claim 13. Accordingly, the 35 U.S.C. 102(b) rejection of Claim 13 over Shen is improper and must be withdrawn.

2) Claim 5 is rejected under 35 U.S.C. § 103(a) as being obvious over Shen et al. in view of Ebrahim et al. (U.S. Patent 5,893,121). Applicants traverse this rejection for the reasons set forth below.

Claim 5 further defines the method of claim 3, wherein the cache memory maintains a single dirty cache line for stack data. Claim 5 is allowable for the same reasons set forth above in support of the allowance of Claim 3. Claim 3 is allowable for

the same reasons set forth above in support of the allowance of Claim 2. Claim 2 is allowable for the same reasons set forth above in support of the allowance of Claim 1. Further, the Examiner admits that, "Shen does not disclose that the cache memory maintains a single dirty cache line for stack data" (Office Action, page 8, paragraph 31). The Examiner relies upon Ebrahim to provide this teaching. Assuming, arguendo, that the Examiner is correct concerning the teaching of Ebrahim, the reference still fails to provide the previously described deficiencies of Shen as related to Claims 1, 2 and 3.

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. (MPEP § 2143). Applicants respectfully submit that Examiner has failed to establish all three criteria. Thus, claim 5 is patentable under 35 U.S.C. § 103(a) over Shen in view of Ebrahim.

3) Claims 6 and 17-20 are rejected under 35 U.S.C. § 103(a) as being obvious over Shen et al. in view of Steely. Applicants traverse this rejection for the reasons set forth below.

Claim 6 further defines the method of claim 3, wherein if a dirty cache line needs to be written back, **then analyzing the trend information**, which includes **determining which word of the dirty cache line is going to be written to.**

Examiner admits that Shen fails to teach or suggest which word of a dirty cache line is going to be written to (Office Action, page 7, lines 17-18). To overcome this omission, Examiner relies upon Steely. However, there is a problem with Steely, since it fails to teach or suggest there is more than one word in a dirty cache line. To overcome this omission, Examiner misconstrues the words of Claim 6 to fit Steely. More particularly, Examiner states:

> It should be noted that when taking the broadest reasonable interpretation of the claim language it is clear that the limitations of the claim do not specify how many words are in a dirty cache line. Steely does not disclose the exact size of a cache line, however, at a minimum it must contain one word, meaning a write request would always go to a predetermined word with a dirty cache line that being **the only word** in the dirty cache line" (Office Action, page 7, line 20 – page 8, line 3).

Examiner thus argues that Steely, which discloses only one word in the dirty cache line anticipates Claim 6's language, "... **then analyzing the trend information**, which includes **determining which word of the dirty cache line is going to be written to**". Applicants respectively point out, however, that the language "**determining which word of the dirty cache line**", implies more than one word in the dirty cache line, one of which is going to be written to. Steely does not teach or suggest more than one word in the dirty cache line. Accordingly, Examiner has not considered all of the words of Claim 6, as is required by law.

Claim 6 is allowable for the same reasons set forth above in support of the allowance of Claim 3. Claim 3 is allowable for the same reasons set forth above in support of the allowance of Claim 2. Claim 2 is allowable for the same reasons set forth above in support of the allowance of Claim 1.

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. (MPEP § 2143). Applicants respectfully submit that Examiner has failed to establish all three criteria. Thus, claim 6 is patentable under 35 U.S.C. § 103(a) over Shen in view of Steely.

Independent Claim 17 requires and positively recites, a method, comprising: "issuing a write request to a cache memory, wherein the cache memory includes multiple cache lines", "determining whether the write request refers to a **predetermined** word within a dirty cache line" and "**determining whether the size of a stack is increasing or decreasing**".

Examiner admits that Shen does not teach or suggest, "issuing a write request to a cache memory, wherein the cache memory includes multiple cache lines" and "determining whether the write request refers to a predetermined word within a dirty cache line". Examiner relies upon Steely to provide these omissions in Shen (Office Action, page 8, lines 19-22).

Examiner admits that Shen fails to teach or suggest which word of a dirty cache line is going to be written to (Office Action, page 7, lines 17-18). To overcome this omission, Examiner relies upon Steely. However, there is a problem with Steely, since it fails to teach or suggest there is more than one word in a dirty cache line. To overcome this omission, Examiner misconstrues the words of Claim 17 to fit Steely. More particularly, Examiner states:

> It should be noted that when taking the broadest reasonable interpretation of the claim language it is clear that the limitations of the claim do not specify how many words are in a dirty cache line. Steely does not disclose the exact size of a cache line, however, at a minimum it must contain one word, meaning a write request would always go to a predetermined word with a dirty cache line that being **the only word** in the dirty cache line" (Office Action, page 7, line 20 – page 8, line 3).

Examiner thus argues that Steely, which discloses only one word in the dirty cache line anticipates Claim 17's language, "determining whether the write request refers to a **predetermined** word within a dirty cache line". Applicants respectively point out, however, that the language ". . . a **predetermined** word within a dirty cache line", implies more than one word in the dirty cache line, one of which could be predetermined. Steely does not teach or suggest more than one word in the dirty cache line AND that a word in the dirty cache line could be predetermined. Accordingly, Examiner has not considered all of the words of Claim 17, as is required by law.

Further, there is no teaching in Shen (col. 3, line 65 - col. 7, line 7; col. 4, lines 11-15 and 36-60; col. 5, lines 1-7 and 9-10; and Fig. 2) for "**determining whether the size of a stack is increasing or decreasing**", as required by Claim 17, as suggested by the Examiner. Even though Shen discloses on col. 3, line 65, a five-stage pipeline, it says nothing about **determining whether the size of a stack is increasing or decreasing**. Similarly, while col. 7, line 7 teaches that the stack valid bits for all three pipelines are set to zero, again, it says nothing about **determining whether the size of a stack is increasing or decreasing**. Further, there is nothing in Fig. 2 that teaches or suggest, **determining whether the size of a stack is increasing or decreasing**". As such, any combination of Steely and Shen fails to teach or suggest, "**determining whether the size of a stack is increasing or decreasing**", as required by Claim 17.

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. (MPEP § 2143). Applicants respectfully submit that Examiner has failed to establish all three criteria. Thus, claim 17 is patentable under 35 U.S.C. § 103(a) over Steely in view of Shen.

Claims 18-20 stand allowable as depending directly, or indirectly, from allowable Claim 17.

Claim 18 further defines the method of claim 17, by further comprising determining whether the write request will be **to the end of a dirty cache line**. Claim 18 stands allowable for the same reasons provided above in support of the allowance of Claim 17.

Claim 19 further defines the method of claim 18, wherein the **stack size is increasing and the dirty cache line is written to a main memory**. Claim 19 stands allowable for the same reasons provided above in support of the allowance of Claim 18.

Claim 20 further defines the method of claim 18, wherein the **stack size is decreasing and the dirty cache line is retained in the cache memory**. Claim 20 stands allowable for the same reasons provided above in support of the allowance of Claim 18.

The Examiner admits that Steely does not disclose that the stack size is increasing (Office Action, page 13, paragraph 40, line 3). The Examiner relies upon Shen as disclosing that the stack size is increasing (Office Action, page 12, paragraph 40, line 4).

However, neither Shen nor Steely teach or suggest that a dirty cache line is written to a main memory when stack size is increasing, as required by Claim 19. Similarly, neither Shen nor Steely teach or suggest that a dirty cache line is retained in the cache memory when stack size is decreasing, as required by Claim 20.

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. (MPEP § 2143). Applicants respectfully submit that Examiner has failed to establish all three criteria. Thus, claims 19 and 20 are patentable under 35 U.S.C. § 103(a) over Steely in view of Shen.

Moreover, obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art. "The test for an implicit showing is what the combined teachings, knowledge of one of ordinary skill in the art, and the nature of the problem to be solved as a whole would have suggested to those of ordinary skill in the art." *In re Kotzab,* 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000). See also *In re Lee,* 277 F.3d 1338, 1342-44, 61 USPQ2d 1430, 1433-34 (Fed. Cir. 2002) (discussing the importance of relying on objective evidence and making specific factual findings with respect to the motivation to combine references); *In re Fine,* 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); *In re Jones,* 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

Examiner fails to offer ANY rationale for combining Shen with Steely. As such, the Examiner has failed to set forth a prima facie case of the obviousness of Claims 19 and 20. As such, the 35 U.S.C. 103(a) rejection of Claims 19 and 20 is improper and must be withdrawn.

4) Claims 12 and 14 are rejected under 35 U.S.C. § 103(a) as being obvious over Shen et al. in view of O'Connor et al. (U.S. Patent 6,026,485). Applicants traverse this rejection for the reasons set forth below.

Claim 12 further defines the computer system of claim 11, further comprising an instruction decoder **comprising a first portion that decodes current instructions and a second portion that decodes future instructions.**

Claim 14 further defines the computer system of claim 12, wherein the **second portion of the decoder is adjusted so that the number of future instructions that are decoded equals at least two.**

Claim 12 is allowable for the same reasons set forth above in support of the allowance of Claim 11. Further, the Examiner admits that, "Shen does not disclose an instruction decoder comprising a first portion that decodes current instructions and a second portion that decodes future instructions" (Office Action, page 11, lines 1-3). The Examiner relies upon O'Connor to provide this teaching. Assuming, arguendo, that the Examiner is correct concerning the teaching of O'Connor, the reference still fails to provide the previously described deficiencies of Shen as related to Claim 11.

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. (MPEP § 2143). Applicants respectfully submit that Examiner has failed to establish all three criteria. Thus, claim 12 is patentable under 35 U.S.C. § 103(a) over Shen in view of O'Connor.

Claim 14 further defines the method of Claim 12, wherein the second portion of the decoder is adjusted so that the number of future instructions that are decoded equals at least two. Claim 14 is allowable for the same reasons set forth in support of the allowance of Claim 12. Claim 12 is allowable for the same reasons set forth above in support of the allowance of Claim 11. Moreover, even if, arguendo, O'Connor were to disclose an instruction decoder comprising a first portion that decodes current instructions and a second portion that decodes future instructions, O'Connor fails to teach the previously described deficiencies of the Shen reference as reflected in Claims 11 and 12.

Objected to Claim 7, 9, 10 15 and 16 have been amended to be allowable. Claim 1 has been amended to overcome the 35 U.S.C. 112, first paragraph, rejection of Claims 1-10. In light of the above amendments and arguments, Claims 1-20 are allowable over the cited references. Applicants respectfully request reconsideration and allowance of the application at the earliest possible date.

Respectfully submitted,

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